What is claimed is:

1. A process comprising:

above a substrate, forming a strained silicon layer above a semiconductive silicon compound layer;

forming a recess in the substrate to laterally isolate the strained silicon; and

vertically isolating the strained silicon layer from the substrate by undercutting.

2. The process according to claim 1, wherein vertically isolating the strained silicon layer precedes forming the strained silicon layer.

3. The process according to claim 1, wherein vertically isolating the strained silicon layer precedes forming the strained silicon layer, and wherein forming a strained silicon layer further includes:

forming the semiconductive silicon compound layer by implanting material in the substrate.

4. The process according to claim 1, wherein vertically isolating the strained silicon layer precedes forming the strained silicon layer, and wherein forming a strained silicon layer further includes:

growing the semiconductive silicon compound layer upon the substrate; and

growing the strained silicon layer upon the semiconductive silicon compound layer.

5. The process according to claim 1, following forming a recess, further including:

forming a gate above the strained silicon layer.

6. The process according to claim 1, wherein vertically isolating further includes:

forming a spacer in the recess; and

isotropically etching in the recess under conditions to undercut the spacer.

7. The process according to claim 1, wherein vertically isolating further includes:

forming a spacer in the recess;

isotropically etching in the recess under conditions to undercut the spacer; and

forming an oxide in the substrate.

8. The process according to claim 1, wherein vertically isolating further includes:

forming a spacer in the recess;

isotropically etching in the recess under conditions to form an undercut at the spacer, and under conditions to cause faceting of the substrate at the undercut.

9. The process according to claim 1, wherein vertically isolating further includes:

forming a spacer in the recess;

isotropically etching in the recess under conditions to undercut the spacer; and

forming an oxide in the semiconductive substrate, the process further including:

filling the recess with a shallow-trench dielectric.

10. The process according to claim 1, wherein forming a strained silicon layer above a semiconductive silicon compound layer includes solid-phase epitaxial formation of the strained silicon layer.

11. A process comprising:

forming a relaxed SiGe layer above a substrate;

forming a strained silicon layer above the relaxed SiGe layer;

forming at least one recess in the substrate to laterally isolate the strained silicon layer; and

vertically isolating the strained silicon layer from the substrate by undercutting.

12. The process according to claim 11, wherein vertically isolating the strained silicon layer precedes forming the strained silicon layer.

13. The process according to claim 11, wherein vertically isolating the strained silicon layer precedes forming the strained silicon layer, and wherein forming the strained silicon layer includes implanting to form the relaxed SiGe layer above the substrate.

14. The process according to claim 11, wherein vertically isolating the strained silicon layer precedes forming the strained silicon layer, and wherein forming the strained silicon layer includes growing the relaxed SiGe layer above the substrate, and growing the strained silicon layer above the relaxed SiGe layer.

15. The process according to claim 11, wherein vertically isolating further includes:

forming a spacer in the at least one recess;

isotropically etching in the at least one recess under conditions to undercut the spacer; and

forming an oxide in the substrate.

16. The process according to claim 11, wherein vertically isolating further includes:

forming a spacer in the at least one recess;

isotropically etching in the at least one recess under conditions to undercut the spacer; and

forming an oxide in the semiconductive substrate, the process further including:

filling the at least one recess with a shallow-trench dielectric.

17. The process according to claim 11, wherein forming a relaxed SiGe layer above a substrate includes forming a graded relaxed SiGe layer.

18. The process according to claim 11, further including:

forming at least one junction in the strained silicon layer; and

forming a storage device above the at least one junction.

19. A process of forming an active area, comprising:

forming a deep implantation in a substrate below a top surface of the substrate;

forming a semiconductive silicon compound layer above the deep implantation;

forming a strained silicon layer above the semiconductive silicon compound layer;

forming a recess in the substrate to laterally isolate the strained silicon; and

vertically isolating the strained silicon layer from the substrate by undercutting.

20. The process according to claim 19, wherein vertically isolating the strained silicon layer includes forming a thermal oxide in the recess that undercuts the strained silicon layer.

21. The process according to claim 19, wherein vertically isolating the strained silicon layer includes:

conducting an undercutting etch in the recess to partially undercut the strained silicon layer; and

forming a thermal oxide in the recess that completely undercuts the strained silicon layer.

22. A process comprising:

forming a recess in a substrate to form an active area precursor;

partially undercutting the active area precursor;

forming an oxide in the undercutting to fully undercut the active area precursor;

forming a semiconductive silicon compound layer above and on the active area precursor;

forming a strained silicon layer above and on the semiconductive silicon compound layer; and

forming at least one junction in the strained silicon layer.

23. The process according to claim 22, wherein forming the strained silicon layer includes ion implantation below the strained silicon layer.

24. The process according to claim 22, wherein forming the strained silicon layer includes growing the strained silicon layer upon a semiconductive silicon compound layer.

25. The process according to claim 22, wherein forming the oxide includes forming a thermal oxide.

26. An article comprising:

a substrate;

a relaxed semiconductive silicon compound layer disposed above the substrate;

a strained silicon layer disposed above the relaxed semiconductive silicon compound layer;

wherein the strained silicon layer is laterally isolated by a shallow trench isolation, and wherein the strained silicon layer is vertically isolated by a thermal oxide.

27. The article according to claim 26, wherein the relaxed semiconductive silicon compound layer includes a SiGe compound.

28. The article according to claim 26, above the strained silicon layer, further including:

a storage device.

29. An electrical device comprising:

a substrate;

a relaxed semiconductive silicon compound layer disposed above the substrate;

a strained silicon layer disposed above the relaxed semiconductive silicon compound layer, wherein the strained silicon layer is laterally isolated by a shallow trench isolation, and wherein the strained silicon layer is vertically isolated by a thermal oxide; and

a gate disposed above the strained silicon layer.

30. The electrical device according to claim 29, further including:

a chip package, wherein the substrate is disposed in the chip package.

31. The electrical device according to claim 29, further including:

a chip package, wherein the substrate is disposed in the chip package; and

a host, wherein the chip package is disposed in the host.

32. The electrical device according to claim 29, further including:

a chip package, wherein the substrate is disposed in the chip package; and

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module.

33. The electrical device according to claim 29, further including:

a chip package, wherein the substrate is disposed in the chip package; and

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module; and

an electronic system, wherein the memory module is disposed in the electronic system.

34. The electrical device according to claim 29, further including:

a chip package, wherein the substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host includes a dynamic random access memory module; and

an electronic system, wherein the dynamic random access memory module is disposed in the electronic system.

35. The electrical device according to claim 29, further including:

a chip package, wherein the substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host; and

an electronic system, wherein the host is disposed in the electronic system.

36. A method of assembling an electrical device comprising:

above a substrate, forming a strained silicon layer above a semiconductive silicon compound layer;

forming a recess in the substrate to laterally isolate the strained silicon;

vertically isolating the strained silicon layer from the substrate by undercutting; and

forming at least one junction in the strained silicon layer.

37. The method according to claim 36, further including:

configuring the strained silicon layer in an array of similar strained silicon layers.

38. The method according to claim 36, further including:

configuring the strained silicon layer in an array of similar strained silicon layers; and

forming a data storage device above the strained silicon layer.

39. The method according to claim 36 further including:

configuring the strained silicon layer in an array of similar strained silicon layers;

forming a data storage device above the strained silicon layer; and

placing the array in a chip package.

40. The method according to claim 36 further including:

configuring the strained silicon layer in an array of similar strained silicon layers;

forming a data storage device above the strained silicon layer;

placing the array in a chip package; and

placing the chip package into a host, wherein the host includes a chip set.

41. The method according to claim 36 further including:

configuring the strained silicon layer in an array of similar strained silicon layers;

forming a data storage device above the strained silicon layer;

placing the array in a chip package;

placing the chip package into a host, wherein the host includes a chip set; and

incorporating the chip set into an electronic system.

42. A computer system, comprising:

a processor;

a memory system coupled to the processor;

an input/output (I/O) circuit coupled to the processor and the memory system; and

a strained silicon on insulator structure disposed in the processor or the memory system, the strained silicon on insulator structure including:

a substrate;

a relaxed semiconductive silicon compound layer disposed above the substrate;

a strained silicon layer disposed above the relaxed semiconductive silicon compound layer;

wherein the strained silicon layer is laterally isolated by a shallow trench isolation, and wherein the strained silicon layer is vertically isolated by a dielectric.

43. The computer system according to claim 42, wherein the dielectric is a thermal oxide.

44. The computer system according to claim 42, wherein the processor is disposed in a host selected from a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and a hand-held.

45. The computer system according to claim 42, wherein the memory system is disposed in a host selected from a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and a hand-held.